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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/655,854	09/05/2003	Rafael Reif	MIT-136AUS	7254

22494 7590 07/27/2005

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EXAMINER	
ANDUJAR, LEONARDO	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/655,854	REIF ET AL.	
	Examiner	Art Unit	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/8*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of species 2 in the reply filed on 05/11/2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the third semiconductor structure according to claim 41 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If

the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 4 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. In the instant case, claim 4 depends on cancelled claim 3.

4. Claim 9 is objected to because of the following informalities: Claim 9 recites in lines 2-3 "the first conductive interconnect" and in line 4 "the first third conductive interconnect". There is insufficient antecedent basis for these limitations in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

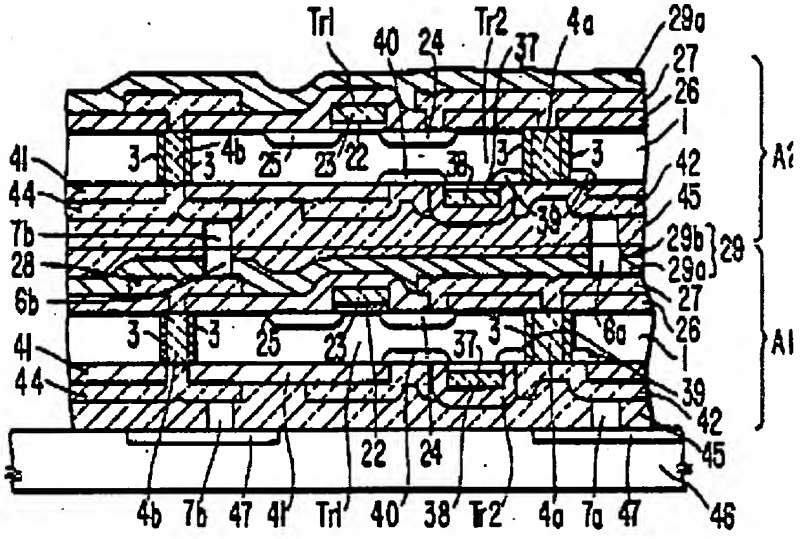
> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 2, 4-13, and 17-41 are rejected under 35 U.S.C. 102(b) as being anticipated by Kato (US 4,939,568)

7. Regarding claim 1, Kato (e.g. fig. 3) show a multi layer integrated semiconductor structure, comprising:

- A first device layer including:
  - A first substrate 1 having provided therein a first plurality of doped regions (24, 25) which from at least part of one or more semiconductors elements (transistor);
  - A dielectric material 29 disposed over the first substrate;
  - And a first conductive via 6a provided in the dielectric material, the first conductive via having a first end and a second end;
- A conductive interface 7b having a first surface disposed over at least a portion of the first device layer such that at least a portion of the conductive interface is couple to at least a portion of the first end of the first conductive via in the first device layer;
- A second device layer disposed over a second surface of the conductive interface, the second device layer including:
  - A second substrate 1 having provided therein a second plurality of doped regions (24, 25) which from at least part of one or more semiconductors elements (transistor);
  - An insulating material (41, 45) having a surface disposed against a second surface of the conductive interface; wherein the second

device layer is secured to the first device layer via the interface; and a second conductive via 4a provided in the second device layer having a first end coupled to the conductive interface and having a second end coupled to at least one of the second plurality of doped regions such that an electrical path between the first device layer and the second device layer is provided by the first conductive via, the conductive interface and the second conductive via.



8. Regarding claim 2, Kato shows a first conductive interconnect element 27 disposed in the dielectric material of the first device layer with a first end of the conductive interconnect element coupled to the first conductive via and a second end of the first conductive interconnect element coupled to at least one of the first plurality of doped semiconductor elements.

9. Regarding claim 4 (assumed to depend on claim 1), Kato shows a second conductive interconnect 27 having a first portion disposed over at least a portion of one

of the second plurality of doped regions and having a second portion coupled to the second end of the second conductive via.

10. Regarding claim 5, Kato shows a second conductive interconnect 27 disposed in the second device layer and coupled to the second conductive via provided in the second device layer.

11. Regarding claim 6, Kato shows that the second conductive interconnect is coupled to at least one of the semiconductor element of the second device layer.

12. Regarding claim 7, Kato shows that the second conductive via includes a first end coupled to the at least one of the one or more semiconductor elements in the second device layer and a second end coupled to the first conductive interface.

13. Regarding claim 8, Kato shows that the second device layer comprises a second conductive interconnect 27 having a first portion coupled to the second conductive via and a second portion coupled to at least one element of the second plurality of semiconductor elements such that the second conductive interconnect couples the second conductive vias to the at least one element of the second plurality of semiconductor elements.

14. Regarding claim 9 (as understood), Kato shows a third conductive interconnect 27 (horizontal portion) disposed over at least a portion of a first conductive interconnect 27(contact plug). Also, the second end of the first conductive via is coupled to the third conductive interconnect.

15. Regarding claim 10, Kato shows a third conductive via 4a provided in the first device layer, wherein the third conductive via is coupled between a portion of the first conductive interconnect and the at least one of the first plurality of doped regions.

16. Regarding claim 11, Kato shows a second conductive interface disposed over a first surface of the second device layer and, wherein the second conductive via forms at least a part of the electrical communication path between the second conductive interconnect and the second interface.

17. Regarding claim 12, Kato shows that the first conductive via forms at least a signal path between the conductive interface and at least one of the first and second plurality of semiconductor elements.

18. Regarding claim 13, Kato shows that the second end of the first conductive via is coupled to the at least one element of the first plurality of semiconductor elements.

19. Regarding claim 17, Kato (e.g. fig. 3) show a multi layer integrated semiconductor structure, comprising:

- A first device layer 1 including:
  - First and second opposing surface
  - A first semiconductor region (24, 25);
  - A first dielectric material 29 disposed about the first doped semiconductor region, the dielectric material having at least a first via hole 6a;
  - A first conductive material 6a disposed in the via hole to provide a first conductive via having first and second opposing ends;

- A second device layer 1 having first and second opposing surfaces including:
  - At least a second doped semiconductor region (24, 25) and including a second via hole 4a; a second conductive material 4a disposed therein to provide a second conductive via having first and second ends;
- A first interface 7a disposed between a first one of the first and second opposing surfaces of the first device layer and a first one of the first and second opposing surfaces of the second device layer such that the first interface secures together the first and second device layers and also electrically couples the first device layer to the second device layer wherein the conductive interface and the first and second conductive vias forms at least a portion of an electrical communication path between the first device layer and the second device layer.

20. Regarding claim 18, Kato shows a first conductive interconnect element 27 disposed in the first layer with a first portion of the first conductive via electrically coupled to at least a portion of the first conductive interconnect element and a second portion of the first conductive interconnect element coupled to the first doped semiconductor region.

21. Regarding claim 19, Kato shows that the first conductive via couples the first conductive interconnect element to the first conductive interface.

22. Regarding claim 20, Kato shows that the second conductive via is formed on the first one of the first and second opposing surfaces of the second device layer and is coupled to the second doped semiconductor region.

23. Regarding claim 21, Kato shows a third conductive via 4a coupled to the second doped semiconductor region.

24. Regarding claim 22, Kato shows a second conductive interface 7a disposed on the second one of the first and second opposing surfaces of the second device layer and wherein the third conductive via is provided having a first end coupled to the second doped semiconductor region and a second end coupled to the second conductive interface.

25. Regarding claim 23, Kato shows that the second conductive via is formed on the first one of the first and second opposing surface of the second device layer and wherein the second device layer comprises a first conductive inter connect 27.

26. Regarding claim 24, Kato shows that the second conductive via is provided having a first end coupled to the conductive interconnect 27 and a second end coupled to the fist conductive interface.

27. Regarding claim 25, Kato shows that the first conductive via is coupled to at least the first doped semiconductor region.

28. Regarding claim 26, Kato shows that the first conductive via is provided having a first end coupled to at least the first doped semiconductor region and a second end coupled to the first conductive interface.

29. Regarding claim 27, Kato shows that the first interface corresponds to a first conductor interface region (right side). Also, a second interface region (left side) is disposed between the first one of the first and second device layers with the second interface region provided from a non-conductive material 29b.

30. Regarding claim 28, Kato shows that the first conductive interface region is provided from a conductive bonding material (e.g. fig. 4f, col. 5/ll. 51).

31. Regarding claim 29, Kato shows a second conductive interconnect element 27 disposed in the second device layer with a portion of the second conductive interconnect element coupled to the second conductive via and wherein the first conductive via, the first conductive interface and the second conductive via provide a direct vertical electrical connection between the first conductive interconnect element and the second conductive interconnect element.

32. Regarding claim 30, Kato shows that the first device layer is constructed and arranged to operate using at least one of electronic components (abstract).

33. Regarding claim 31, Kato shows that the second device layer is constructed and arranged to operate using at least one of electronic components (abstract).

34. Regarding claim 32, Kato shows that the first device layer includes a transistor.

35. Regarding claim 33, Kato shows that the second device layer includes a transistor.

36. Regarding claims 34 and 35, Kato shows that the first and second device layers includes a die element (transistor) located on a wafer (col. 7/lls. 43-35).

37. Regarding claim 36, Kato shows that the first device layer includes a first predetermined surface area and the second device layer includes a second predetermined surface area whereby the first predetermined surface area differs from the second predetermined surface area.

38. Regarding claim 37, Kato shows that the first device layer includes a first predetermined surface area and the second device layer includes a second predetermined surface area is substantially equivalent to the first predetermined surface area.

39. Regarding claim 38, Kato shows a first conductive interconnect element 27 having a first portion coupled to the first doped semiconductor region, and a second portion coupled to a first end of the first conductive via.

40. Regarding claim 39, Kato shows a second conductive interconnect element 27 having a first portion coupled to the second doped semiconductor region and a second portion coupled to a first end of the second conductive via with the second end of the first conductive via and the second end of the second conductive via each coupled to the first interface.

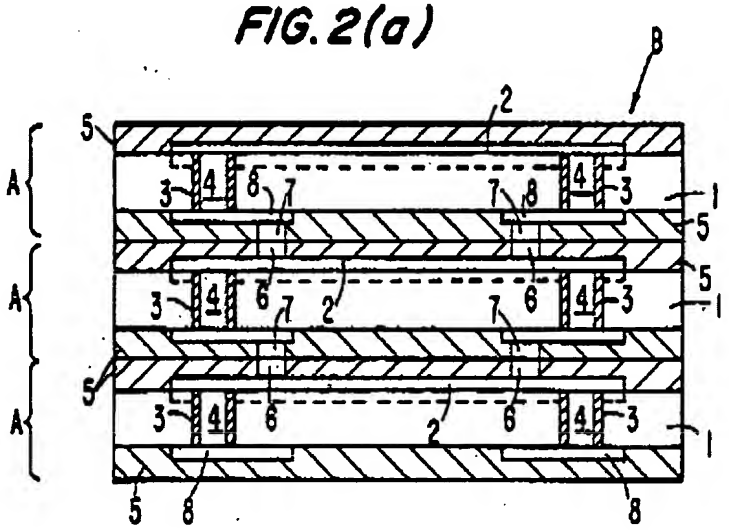
41. Regarding claim 40, Kato (e.g. fig. 3) shows a multi layer integrated semiconductor structure, comprising: a first semiconductor wafer 1 including a plurality of semiconductor structures (transistors) each of which includes a first plurality of semiconductor elements (24, 25, 27); a second semiconductor wafer 1 including a second plurality of semiconductor structures (transistors) each of which includes a second plurality of semiconductor elements (24, 25, 27); and at least a first conductive

bonding interface segment 7b disposed between the first and second semiconductor wafers; the first conductive bonding interface segment disposed over at least a first one of the plurality of semiconductor structures of the first semiconductor wafer and being in an electrical communication relationship with at least a first one of the first plurality of the semiconductor elements of the first semiconductor structure and; first one of the plurality of semiconductor elements of the second semiconductor structure of the second semiconductor wafer where the first conductive bonding interface segment permits at least the first semiconductor element of the first semiconductor structure to communicate with at least the second semiconductor element of the second semiconductor structure.

42. Regarding claim 41, Kato shows (e.g. figs. 2a and 3) shows a multi layer semiconductor structure, comprising: at least a first semiconductor structure 1 including a first plurality of conductive elements 4; at least a second semiconductor structure 1 including a second plurality of conductive elements 4; a first plurality of conductive bonding interface segments 7 disposed between the first and second semiconductor structures with each of the plurality of conductive bonding interface segments being in an electrical communication relationship with one or more of the conductive elements of the first semiconductor structure and one or more of the conductive elements of the second semiconductor structure; at least a third semiconductor structure 1 including a third plurality of conductive elements 4 and a second plurality of conductive bonding interface 7 disposed between the second and third semiconductor structures with each of the second plurality of conductive bonding interface segments being in electrical

communication relationship with one or more of the conductive elements of the second semiconductor structure and one or more of the conductive elements of the third semiconductor structure.

FIG. 2(a)

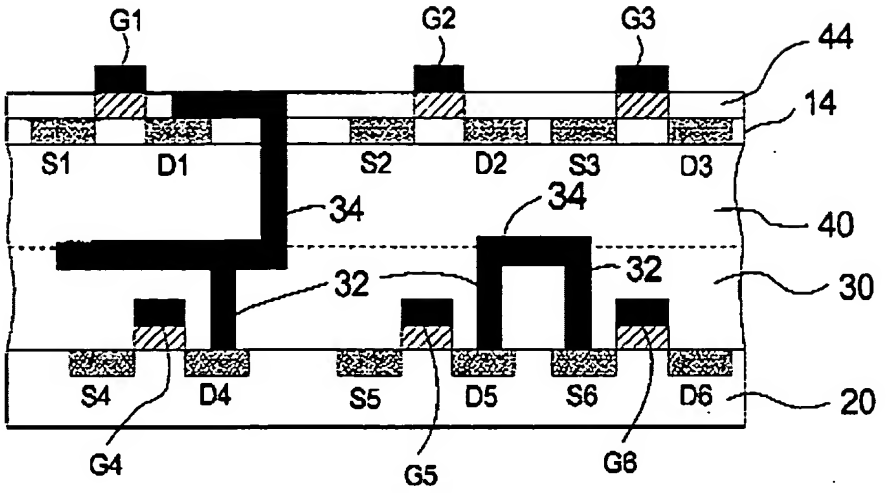


43. Claims 1, 2, 4-8, 12, 13 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Tiwari (US 6,600,173)

44. Regarding claim 1, Tiwari (e.g. fig. 7) show a multi layer integrated semiconductor structure, comprising:

- A first device layer including:
  - A first substrate 20 having provided therein a first plurality of doped regions (S4, D4) which from at least part of one or more semiconductors elements (transistor);
  - A dielectric material 30 disposed over the first substrate;
  - And a first conductive via 32 provided in the dielectric material, the first conductive via having a first end and a second end;

- A conductive interface 34 (horizontal layer) having a first surface disposed over at least a portion of the first device layer such that at least a portion of the conductive interface is couple to at least a portion of the first end of the first conductive via in the first device layer;
- A second device layer disposed over a second surface of the conductive interface, the second device layer including:
    - A second substrate 14 having provided therein a second plurality of doped regions (S1, D1) which from at least part of one or more semiconductors elements (transistor);
    - An insulating material 40 having a surface disposed against a second surface of the conductive interface; wherein the second device layer is secured to the first device layer via the interface; and a second conductive via 34 (vertical section) provided in the second device layer having a first end coupled to the conductive interface and having a second end coupled to at least one of the second plurality of doped regions such that an electrical path between the first device layer and the second device layer is provided by the first conductive via, the conductive interface and the second conductive via.



45. Regarding claim 4 (assumed to depend on claim 1), Tiwari shows a second conductive interconnect 34 (top horizontal layer) having a first portion disposed over at least a portion of one of the second plurality of doped regions (e.g. D1) and having a second portion coupled to the second end of the second conductive via.

46. Regarding claim 5, Tiwari shows a second conductive interconnect 34 (top horizontal layer) disposed in the second device layer and coupled to the second conductive via provided in the second device layer.

47. Regarding claim 6, Tiwari shows that the second conductive interconnect is coupled to at least one of the semiconductor element (e.g. D1) of the second device layer.

48. Regarding claim 7, Tiwari shows that the second conductive via includes a first end coupled to the at least one of the one or more semiconductor elements in the second device layer and a second end coupled to the first conductive interface.

49. Regarding claim 8, Tiwari shows that the second device layer comprises a second conductive interconnect (top horizontal layer) having a first portion coupled to

the second conductive via and a second portion coupled to at least one element of the second plurality of semiconductor elements such that the second conductive interconnect couples the second conductive vias to the at least one element of the second plurality of semiconductor elements.

50. Regarding claim 12, Tiwari shows that the first conductive layer via forms at least a signal path between the conductive interface and at least one of the first and second plurality of semiconductor elements.

51. Regarding claim 13, Tiwari shows that the second end of the first conductive via is coupled to the at least one element of the first plurality of semiconductor elements.

52. Regarding claim 17, Tiwari (e.g. fig. 7) show a multi layer integrated semiconductor structure, comprising:

- A first device layer 20 including:
  - First and second opposing surface
  - A first semiconductor region (S4, D4);
  - A first dielectric material 30 disposed about the first doped semiconductor region, the dielectric material having at least a first via hole 32;
  - A first conductive material 32 disposed in the via hole to provide a first conductive via having first and second opposing ends;
- A second device layer 14 having first and second opposing surfaces including:

- At least a second doped semiconductor region (S1, D1) and including a second via hole 34; a second conductive material 34 disposed therein to provide a second conductive via having first and second ends;

1. A first interface 34 (horizontal layer) disposed between a first one of the first and second opposing surfaces of the first device layer and a first one of the first and second opposing surfaces of the second device layer such that the first interface secures together the first and second device layers and also electrically couples the first device layer to the second device layer wherein the conductive interface and the first and second conductive vias forms at least a portion of an electrical communication path between the first device layer and the second device layer.

Claim Rejections - 35 USC § 103

53. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

54. Claims 7-11 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Kato (US 4,939,568) in view of Nulman (US 5,904,562).

55. Regarding claim 14, Kato shows most aspects of the instant invention except for the use of copper to make the first conductive interface. Nevertheless, Nulman teaches that copper is a suitable material to make metallization films (col. 1/lls. 28-38). It would have been obvious to one having ordinary skill in the art at the time the invention was

made to make the first conductive interface (film metallization) disclosed by Kato of copper as taught by Nulman, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416*

56. Regarding claim 7, Kato shows that the second conductive via includes a first end coupled to the at least one of the one or more semiconductor elements in the second device layer and a second end coupled to the first conductive interface.

57. Regarding claim 8, Kato shows that the second device layer comprises a second conductive interconnect 27 having a first portion coupled to the second conductive via and a second portion coupled to at least one element of the second plurality of semiconductor elements such that the second conductive interconnect couples the second conductive vias to the at least one element of the second plurality of semiconductor elements.

58. Regarding claim 9 (as understood), Kato shows a third conductive interconnect 27 (horizontal portion) disposed over at least a portion of a first conductive interconnect 27(contact plug). Also, the second end of the first conductive via is coupled to the third conductive interconnect.

59. Regarding claim 10, Kato shows a third conductive via 4a provided in the first device layer, wherein the third conductive via is coupled between a portion of the first conductive interconnect and the at least one of the first plurality of doped regions.

60. Regarding claim 11, Kato shows a second conductive interface disposed over a first surface of the second device layer and, wherein the second conductive via forms at

least a part of the electrical communication path between the second conductive interconnect and the second interface.

61. Regarding claim 15, Kato shows that the conductive interface is provided as first conductive interface region (right region) and the multi layer integrated semiconductor structure further comprises a second interface region (left region) disposed between the firstand second device with the second conductive interface region being physically separated from the first conductive interface region.

62. Regarding claim 16, Kato shows that the second interface region includes an adhesive material (e.g. 29b) such that the second interface region secures the first device layer to the second device layer.

63. Claims 7, 8 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tiwari (US 6,600,173) in view of Nulman (US 5,904,562).

64. Regarding claim 14, Tiwari shows most aspects of the instant invention except for the use of copper to make the first conductive interface. Nevertheless, Nulman teaches that copper is a suitable material to make metallization films (col. 1/lls. 28-38). It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the first conductive interface (film metallization) disclosed by Tiwari of copper as taught by Nulman, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416*

65. Regarding claim 7, Tiwari shows that the second conductive via includes a first end coupled to the at least one of the one or more semiconductor elements in the second device layer and a second end coupled to the first conductive interface.

66. Regarding claim 8, Tiwari shows that the second device layer comprises a second conductive interconnect (top horizontal layer) having a first portion coupled to the second conductive via and a second portion coupled to at least one element of the second plurality of semiconductor elements such that the second conductive interconnect couples the second conductive vias to the at least one element of the second plurality of semiconductor elements.

Remarks

67. It not clears if claims 7-11 have be rejected under35 USC § 102 and 35 USC § 103 because it is not clear if claim 7 depend on claim 1 or claim 14.

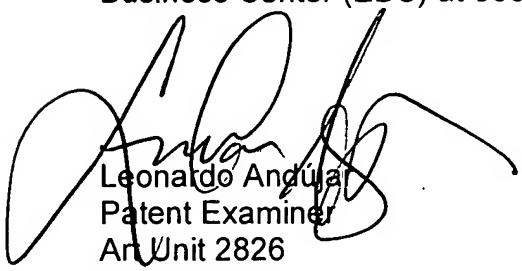
Conclusion

68. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Koyanagi, Hubner, Matshushita and Sugahara teach structures similar to the instant invention.

69. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

70. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

71. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Leonardo Andújar
Patent Examiner
Art Unit 2826
07/21/2005